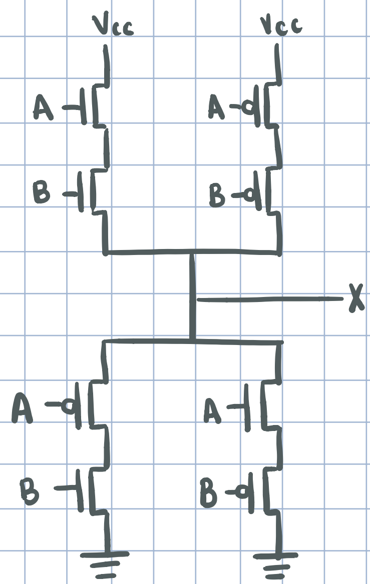
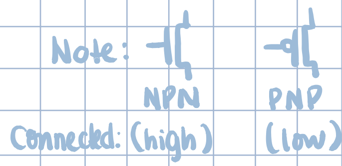
B58 Midterm Seminar

Q1 Draw a circuit (build from transistors) for a XNOR

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1





Q2 Consider the verilog code below:

```
module mystery (A, B, Clk, C, D):
    input A, B, Clk;
    output reg C, D;

    always @ (A, B, Clk)
      if (Clk & (A|B))
        begin
        if (A& ~B)
           D=1;
        else
           D=0;
        if (B & ~A)
           C=1
        else
           C=0;
        end
 endmodule
```

Consider clk is high:

A	B	A|B	D: A&~B	C: B&~A
0	0	0	–	–
0	1	1	0	1
1	0	1	1	0
1	1	1	0	0

Briefly explain what it does:

The module controls the latches C and D that changes only when clock is high. When only B is high, C will be set to high and D to low. When only A is high, D will be set to high and C to low.

When both A and B are low, nothing will happen, so the values of C and D will not change. When both A and B are high both C and D will reset to 0

This module is similar to an S-R latch (A is set, B is reset, D is Q, C is $\bar{Q}$)

Q3 Consider the circuit description given below:

If A is high, we want X to have the same value as B, if A is off and C and D are both high, X should be on. Y acts as A XOR B whenever C is high.

(a) Draw the truth table

A	B	C	D	X	Y
0	0	0	0	x	x
0	0	0	1	x	x
0	0	1	0	x	0
0	0	1	1	1	0
0	1	0	0	x	x
0	1	0	1	x	x
0	1	1	0	x	1
0	1	1	1	1	1
1	0	0	0	0	x
1	0	0	1	0	x
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	x
1	1	0	1	1	x
1	1	1	0	1	0
1	1	1	1	1	0

(b) Use K-map reduction to produce a SOM expression of X and a POM expression for Y. Show your work.

SOM X

	$\bar{A}\cdot\bar{B}$	$\bar{A}\cdot B$	$A\cdot B$	$A\cdot\bar{B}$
$\bar{C}\cdot\bar{D}$	X	X	1	0
$\bar{C}\cdot D$	X	X	1	0
$C\cdot D$	1	1	1	0
$C\cdot\bar{D}$	X	X	1	0

$X = B + \bar{A}$

POM Y

	$\bar{A}+\bar{B}$	$\bar{A}+B$	$A+B$	$A+\bar{B}$
$\bar{C}+\bar{D}$	X	X	X	X
$\bar{C}+D$	X	X	X	X
$C+D$	0	1	0	1
$C+\bar{D}$	0	1	0	1

$Y = (\bar{A}+\bar{B})\cdot(A+B)$

Q4 Calculate $-13d * -7d$ using booth's algorithm. Show your work.

00	No opp
01	Add
10	Subs
11	No opp.

$X = -7d = -(\underbrace{00111b}_{-X}) = 11001b$

$Y = -13d = -(\underbrace{01101b}_{-Y}) = 10011b$

Let P = 00000 00000

$x_0 = 110010$ Substract Y from P's most significant digits

⇒ P = 01101 00000

Arith. Shift right

A. Shift right

⇒ P = 00110 10000

$x_1 = 111001$ Add Y to P's most significant digits.

$$\begin{array}{r} 00110\ 10000 \\ +\ 10011 \\ \hline \end{array}$$

⇒ P = 11001 10000

A. Shift right

A. Shift right

⇒ P = 11100 11000

$x_2 = 111100$ No opperation

A. Shift right

A. Shift right

⇒ P = 11110 01100

$x_3 = 111110$ Substract Y from the most significant digits.

$$\begin{array}{r} 11110\ 01100 \\ +\ 01101 \\ \hline \end{array}$$

⇒ P = 01011 01100

A. Shift right

A. Shift right

⇒ P = 00101 10110

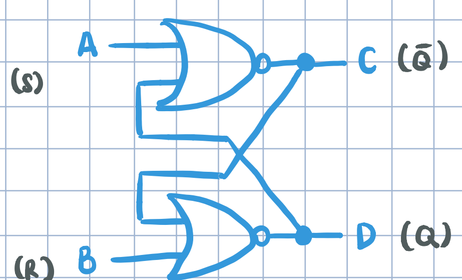
$x_4 = 111111$ No opperation

A. Shift right

⇒ P = 00010 11011

∴ $-13d \times -7d = 00010\ 11011b = 91d$

Q5 Complete the temporal truth table (time going down) for the given circuit



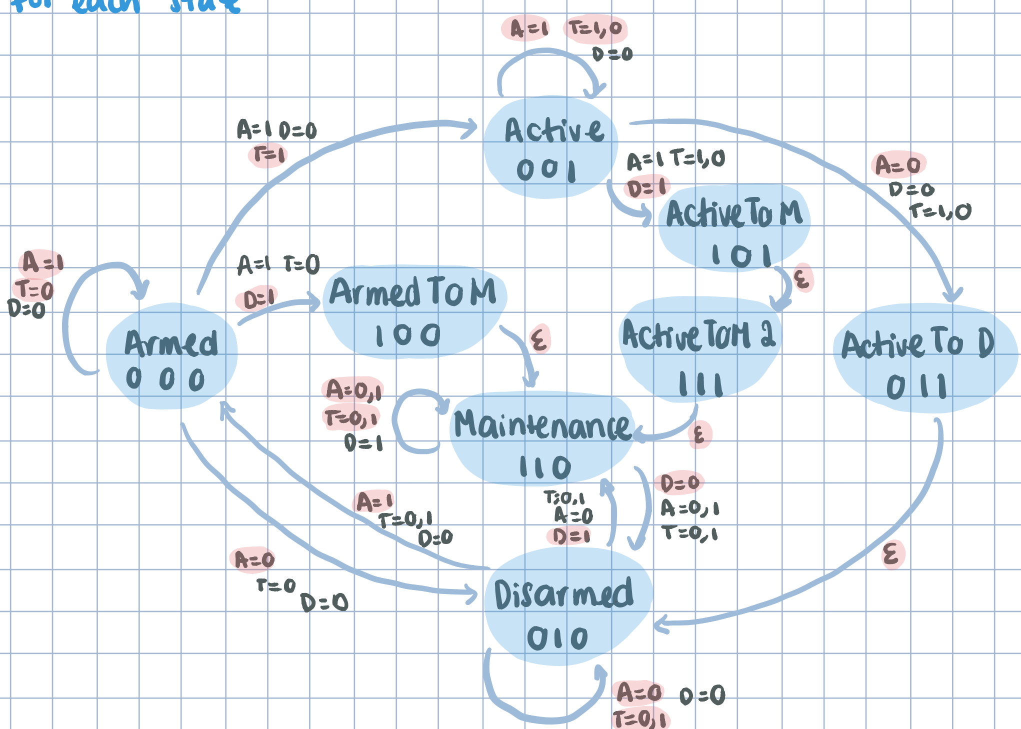
time	A	B	C	D
0	0	0	?	?
1	0	1	1	0
2	0	0	1	0
3	1	0	0	1
4	0	1	1	0

A	B	ANORB
0	0	1
0	1	0
1	0	0
1	1	0

Q6 Consider the system described below:

The alarm system can be toggled between armed and disarmed mode by flipping the 'arm/disarm' switch. In armed mode, if the alarm is tripped, it will go into active mode causing a siren to sound. The alarm shouldn't do anything in disarmed mode. when the system is in active mode, it will put it back into disarmed mode. Also, there is a debug switch which will put it into maintenance mode no matter what it's currently doing. Once the debug switch is turned off, the system goes into disarmed mode.

Draw the FSM diagram for this system, and give the flip-flop assignment for each state



A = Arm
T = Alarm
D = Debug

Previous			A	T	D	Current		
0	0	0	1	1	0	0	0	1
0	0	1	1	1	1	1	0	1
			⋮					